Please check that this question paper contains ___9___ questions and ___2___ printed pages within first ten minutes.

[Total No. of Questions: 09]                              [Total No. of Pages: ..2....]
Uni. Roll No. ...............
                              Program: B.Tech. (Batch 2018 onward)
                              Semester: 3
                              Name of Subject: Digital Circuits and Logic Design
                              Subject Code: ESIT-101
                              Paper ID: ; ·· *16042*

**Time Allowed: 03 Hours**                              **Max. Marks: 60**

**NOTE:**

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

### Part – A                              [Marks: 02 each]

**Q1.**

a) What is De-Morgan's Theorem? (LOTS)

b) What is decoder? Compare decoder and demultiplexer with suitable block diagram. (LOTS)

c) Explain the term resolution and accuracy of A/D convertors. (LOTS)

d) What is the difference between a latch and a flip flop. (LOTS)

e) Perform Subtraction using 2's Complement: $(101001)_2 - (001100)_2$ (HOTS)

f) Add the following decimal numbers using BCD Addition and verify your result: 599 and 984 (HOTS)

### Part – B                              [Marks: 04 each]

**Q2.** Minimize the following expressions using Boolean algebra: (LOTS)

1) $A'.B.C + A.B'.C + A.B.C' + ABC$

2) $(ABC)' (A + C) (A + C')$

**Q3.** Implement full adder using two half adders and one OR gate. (LOTS)

**Q4.** What is Race around condition? How it can be avoided? Also discuss the working of Master Slave J-K Flip Flop. (LOTS)

**Q5.** Explain the working of 3-bit shift register. (HOTS)

**Q6.** Design 4-to-16 decoder with 2-to-4 decoder. (HOTS)

P.T.O.

**Q7.** Draw the circuit of BCD adder and explain it. (HOTS)

<div align="center">

**Part – C**                 **[Marks: 12 each]**

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**Q8.** Simplify the minterm expression for F : $F(P,Q,R,S) = \sum (\ 0,2,5,7,8,10,13,15\ )$ using K-Map. The minterms 2, 7, 8 and 13 are 'do not care' terms. (LOTS)

<div align="center">OR</div>

What are universal gates and why they are called so? Impement AND, OR, NOT and XOR gates using NAND gates. (LOTS)

**Q9.** Design a combinational circuit to implement a 4-bit Binary to Gray code convertor. (HOTS)

<div align="center">OR</div>

Differentiate between synchronous and asynchronous counters. Design 3-bit synchronous up counter using T flip flops. (HOTS)

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